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What is claimed and desired to be secured by United States Letters Patent is:

1. A method for forming an oxide region on a substrate assembly, the method comprising:
  - bombarding a (selected) region of a volume of semiconductor material substantially composed of a first material with ions of said first material, said volume of semiconductor material substantially composed of said first material being situated on a substrate assembly; and
  - oxidizing said first material in said selected region.
2. A method as recited in Claim 1, wherein bombarding a selected region of a volume of semiconductor material substantially composed of a first material with ions of said first material leaves unaltered the electrical charge characteristics of the first material within the selected region.
3. A method as recited in Claim 2, wherein the ions of said first material comprise silicon ions.
4. A method as recited in Claim 3, wherein said first material is substantially composed of monocrystalline silicon.
5. A method as recited in Claim 1, further comprising:
  - forming a hard mask on a top surface of the volume of semiconductor material prior to <sup>Ca<sub>1</sub>b</sup> bombarding a selected region of a volume of semiconductor material substantially composed of a first material with ions of said first material; and

1 subsequently forming an opening in the hard mask to expose the selected  
2 region, the ions of said first material being implanted through the opening in the  
3 hard mask into the selected region.

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5 6. A method as recited in Claim 5, further comprising forming a spacer around  
6 the opening of the hard mask, said spacer extending from the volume of semiconductor  
7 material substantially composed of the first material to make contact with the hard mask,  
8 wherein bombarding a selected region of a volume of semiconductor material substantially  
9 composed of a first material with ions of said first material implants said ions of said first  
10 material immediately adjacent to but not through the spacer around the opening in the hard  
11 mask.

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13 7. A method as recited in Claim 6, wherein forming a spacer around the opening  
14 of the hard mask further comprises:

15 depositing a layer of spacer material over the opening in the hard mask; and  
16 anisotropically etching the layer of spacer material over the opening in the  
17 hard mask to form the spacer around the opening in the hard mask.

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19 8. A method as recited in Claim 7, wherein the layer of spacer material is  
20 (composed) of silicon nitride.

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22 9. A method as recited in Claim 7, wherein the spacer is one of a pair of spacers  
23 through which the ions of said first material are implanted between but not through the pair  
24 of spacers around the opening in the hard mask and into the selected region, wherein the  
25 selected region is situated between the pair of spacers.  
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1 10. A method as recited in Claim 9, wherein the pair of spacers are separated by  
2 a distance in the range from about 0.05 micrometers to about 0.1 micrometers.

3  
4 11. A method as recited in Claim 1, further comprising the steps, prior to  
5 <sup>aid</sup> bombarding a selected region of a volume of semiconductor material substantially composed  
6 of a first material with ions of said first material, of:

7 forming a pad oxide layer over the volume of semiconductor material  
8 substantially composed of the first material;

9 forming a nitride layer over the pad oxide layer;

10 forming a photoresist mask over the nitride layer; and

11 selectively removing the nitride layer through the photoresist mask to expose  
12 an opening to the volume of semiconductor material substantially composed of the  
13 first material at the selected region, wherein the first material is oxidized in the  
14 selected region within the opening to the volume of semiconductor material  
15 substantially composed of the first material.

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17 12. A method as recited in Claim 11, wherein the photoresist mask is removed  
18 after <sup>aid</sup> bombarding a selected region of a volume of semiconductor material substantially  
19 composed of a first material with ions of said first material.

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21 13. A method as recited in Claim 11, wherein <sup>aid</sup> selectively removing the nitride  
22 layer through the photoresist mask includes selectively removing the nitride layer <sup>aid</sup> (through  
23 the pad oxide layer).

1 14. A method as recited in Claim 1, wherein the substrate assembly is oriented  
2 in a (major plane) and the ions of said first material are implanted into the selected region in  
3 a direction that is within ten degrees from a direction that is orthogonal to the major plane  
4 of the substrate assembly.

5  
6 15. A method as recited in Claim 1, wherein <sup>oxidizing</sup> said first material in said  
7 selected region further comprises heating the substrate assembly while exposing the substrate  
8 assembly to oxygen.

9  
10 16. A method as recited in Claim 1, wherein the volume of semiconductor  
11 material substantially composed of said first material is composed of a monocrystalline  
12 material having a lattice structure, wherein the implanted ions of said first material in the  
13 monocrystalline material cause the lattice structure of the monocrystalline material to  
14 become partially randomized at the selected region into which the ions of said first material  
15 are implanted.

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17 17. A method as recited in Claim 16, wherein both the monocrystalline material  
18 and the ions of said first material are substantially composed of silicon.

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20 18. A method as recited in Claim 1, wherein oxidizing said first material in said  
21 selected region is conducted at a pressure in the range of about 1 to 25 atmospheres.

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23 19. A method as recited in Claim 1, wherein oxidizing said first material in said  
24 selected region is conducted at a pressure in the range of about 5 to 25 atmospheres.

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1 20. A method for forming an oxide region on a substrate assembly, the method  
2 comprising the steps of:

3 forming a hard mask over a volume of silicon of a substrate assembly;

4 forming an opening in the hard mask to expose a (selected) region of the  
5 volume of silicon;

6 bombarding the selected region of the volume of silicon with silicon ions  
7 through the opening in the hard mask so as to leave unaltered the electrical charge  
8 characteristics of the selected region of the volume of silicon; and

9 oxidizing the volume of silicon to form silicon dioxide substantially only at  
10 the selected region by exposure of the selected region to oxygen.

11  
12 21. A method as recited in Claim 20, further comprising forming a spacer around  
13 the opening in the hard mask, said spacer extending from the volume of silicon to contact the  
14 hard mask, wherein <sup>6.6.2</sup> bombarding the selected region of the volume of silicon with silicon ions  
15 through the opening in the hard mask implants ions immediately adjacent to but not through  
16 the spacer around the opening in the hard mask.

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18 22. A method as recited in Claim 21, wherein <sup>6.6.2</sup> forming a spacer around the  
19 opening in the hard mask comprises:

20 depositing layer of spacer material over the opening in the hard mask; and

21 anisotropically etching the layer of spacer material at the opening in the hard  
22 mask to form the spacer situated around the opening of the hard mask.

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24 23. A method as recited in Claim 21, wherein the spacer around the opening in  
25 the hard mask is composed of silicon nitride.  
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1           24. A method as recited in Claim 21, wherein the spacer is one of a pair of  
2 spacers, the ions being implanted in between but not through the pair of spacers and past the  
3 hard mask into the selected region of the volume of silicon, and wherein the selected region  
4 is situated between the pair of spacers, whereby the silicon dioxide is not substantially  
5 formed underneath the pair of spacers.

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7           25. A method as recited in Claim 24, wherein the pair of spacers are separated by  
8 a distance in the range of about 0.05 micrometers to about 0.1 micrometers.

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10          26. A method as recited in Claim 20, further comprising forming a pad oxide  
11 layer upon the volume of silicon prior to forming a hard mask over a volume of silicon of  
12 a substrate assembly, the hard mask being formed upon the pad oxide layer, and forming a  
13 hard mask over a volume of silicon of a substrate assembly comprising:

14               forming the hard mask upon the pad oxide layer; and

15               forming a photoresist mask over the hard mask; and wherein silicon dioxide  
16 is formed in the volume of silicon at the selected region beneath the opening in the  
17 hard mask.

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19          27. A method as recited in Claim 26, wherein the photoresist mask is removed  
20 after the step of implanting ions.

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22          28. A method as recited in Claim 26, wherein etching the hard mask also etches  
23 through the pad oxide layer.

1           29.   A method as recited in Claim 20, wherein the substrate assembly is oriented  
2 within a (major plane) and wherein bombarding the selected region of the volume of silicon  
3 with silicon ions through the opening in the hard mask is conducted such that the direction  
4 that the ions are implanted into the selected region is substantially orthogonal to the major  
5 plane of the substrate assembly.

6  
7           30.   A method as recited in Claim 20, wherein oxidizing the volume of silicon to  
8 form silicon dioxide substantially only at the selected region by exposure of the selected  
9 region to oxygen further comprises heating the substrate assembly while exposing the  
10 substrate assembly to oxygen.

11  
12           31.   A method as recited in Claim 20, wherein the volume of silicon is  
13 substantially composed of monocrystalline silicon having a lattice structure, and wherein the  
14 implanted silicon ions in the monocrystalline silicon cause the lattice structure of the  
15 monocrystalline silicon to become partially randomized at the selected region into which the  
16 ions are implanted.



1 32. A method for forming an oxide region on a substrate assembly, the method  
2 comprising the steps of:

3 forming a hard mask over a pad oxide layer situated on a volume of silicon  
4 of a substrate assembly, the substrate assembly being oriented within a (major plane);

5 forming an opening in the hard mask to expose a (selected) region of the  
6 volume of silicon, said selected region of said volume of silicon being substantially  
7 composed of monocrystalline silicon having a lattice structure;

8 depositing layer of silicon nitride over the opening of the hard mask;

9 anisotropically etching the hard mask at the opening in the hard mask to form  
10 a pair of silicon nitride spacers situated on opposite sides of the opening of the hard  
11 mask, each said silicon nitride spacer extending from the volume of silicon to  
12 contact the hard mask;

13 implanting silicon ions between but not through the pair of silicon nitride  
14 spacers and through the opening in the hard mask into the (selected) region of the  
15 volume of silicon such that the direction that the silicon ions are implanted into the  
16 selected region is substantially orthogonal to the major plane of the substrate  
17 assembly, wherein the implanted silicon ions do not substantially alter the electrical  
18 charge characteristic of the (selected) region, and wherein the implanted silicon ions  
19 in the monocrystalline silicon in the (selected) region cause the lattice structure  
20 thereof to become partially randomized; and

21 heating the substrate assembly while exposing the substrate assembly to  
22 oxygen so as to form silicon dioxide at the selected region, whereby the silicon layer  
23 oxidizes faster where the silicon ions are implanted than where the silicon ions are  
24 not implanted.

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33. A method as recited in Claim 32, wherein the pair of spacers are separated by a distance in the range of about 0.05 micrometers to about 0.1 micrometers.

1           34. A method for forming a trench isolation region on a substrate assembly, the  
2 method comprising:

3               forming a trench in a volume of semiconductor material substantially  
4 composed of a first material, said volume of semiconductor material being situated  
5 within a substrate assembly;

6               implanting ions of said first material into a surface of said trench;

7               oxidizing the surface of the trench by exposure thereof to oxygen to form a  
8 thermal oxide layer substantially composed of an oxide of said first material; and

9               filling the remainder of the trench with an insulating material.

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11           35. A method as recited in Claim 34, wherein the ions of said first material  
12 comprise silicon ions.

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14           36. A method as recited in Claim 35, wherein the first material is substantially  
15 composed of monocrystalline silicon.

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17           37. A method as recited in Claim 34, wherein the substrate assembly is oriented  
18 within a (major plane) and <sup>said</sup> implanting ions of said first material is conducted such that the  
19 direction that the ions are implanted into the selected region is within ten degrees from a  
20 direction that is orthogonal to the major plane of the substrate assembly.

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22           38. A method as recited in Claim 34, wherein <sup>said</sup> forming a trench in a volume of  
23 semiconductor material substantially composed of a first material is conducted as a single  
24 etching process that etches (adjacent and substantially contiguous) nitride, oxide, and silicon  
25 layers.  
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39. A method as recited in Claim 34, wherein <sup>said</sup> oxidizing the surface of the trench is conducted at a pressure in the range of about 5 to 25 atmospheres.

40. A method as recited in Claim 34, wherein <sup>said</sup> forming a trench in a volume of semiconductor material substantially composed of a first material comprises:

forming a thin oxide layer on the in a volume of semiconductor material within the substrate assembly;

forming a layer of silicon nitride over the thin oxide layer;

forming a photoresist mask over the layer of silicon nitride; and

conducting a (single etching process) employing multiple etch recipes to etch the silicon nitride layer, the thin oxide layer, and the silicon substrate to form the trench.

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41. A method for forming a (shallow) trench isolation region on a substrate assembly, the method comprising:

forming a trench in a volume of monocrystalline silicon within a substrate assembly;

implanting silicon ions into a surface of the trench;

oxidizing the surface of the trench by exposure of the trench to oxygen so as to form silicon dioxide on the surface of the trench; and

filling the trench with silicon dioxide.

- 1 42. A method for forming a (shallow) trench isolation region on a substrate  
2 assembly, the method comprising:  
3 forming a (thin) oxide layer on a volume of silicon of a substrate assembly;  
4 forming a layer of silicon nitride over the thin oxide layer;  
5 forming a patterned photoresist mask over the layer of silicon nitride;  
6 conducting an etching process that employs multiple etch recipes to etch the  
7 adjacent silicon nitride layer, the thin oxide layer, and the volume of silicon to form  
8 a trench in the volume of silicon;  
9 implanting silicon ions into the trench, the silicon ions being implanted in a  
10 direction that is within ten degrees from a direction that is orthogonal to a plane of  
11 the substrate assembly;  
12 oxidizing the surface of the trench by exposing thereof to oxygen at a  
13 pressure in the range of about 5 to 10 atmospheres so as to form a thermal oxide  
14 layer in the trench;  
15 filling the remainder of the trench with silicon dioxide; and  
16 removing the silicon nitride layer.
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